A Circuit Topology for Microwave Modeling of Plastic Surface Mount Packages

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Abstract—**A circuit topology is described for modeling a class of plastic surface mount packages. The model consists of three pieces each of which is circuit modeled based on an electromagnetic simulation. The resulting parts of the model can then be interconnected with each other and with the model of the monolithic microwave/millimeter wave integrated circuit (MMIC) to be packaged. Various interconnections and grounding schemes can be investigated without resorting to further electromagnetic simulation. The circuit model topology is verified by circuit simulating two simple packaged test circuits and comparing the results to a full electromagnetic simulation. The resulting S parameters are in good agreement over a wide range of frequencies and for a variety of grounding configurations.**

I. Introduction

THE USE OF plastic surface mount packages for microwave integrated circuits (IC's) has burgeoned in recent years due to the demand for low cost components. At present such packages have primarily been used up to 2.4 GHz. However, designing monolithic microwave/millimeter wave integrated circuits (MMIC's) for use in such packages is difficult due to the poor grounding characteristics of the elevated paddle (the MMIC ground) and due to the lack of generally applicable circuit models for the package. This difficulty is exacerbated for designs at higher frequencies and for packages with high pin count and multiple MMIC's.

Fig. 1(a) shows a diagram of an eight lead plastic package. A MMIC is grounded by soldering it to the rectangular paddle in the center of the structure. The paddle ground is electrically connected to the motherboard ground using several of the leads shown in the figure. Grounding leads are connected to the paddle by wire bond or by making them one piece with the paddle. The MMIC RF leads and power supply leads are wire bonded to the MMIC and the entire assembly is encapsulated in plastic.

In previous work, Ndagijimata *et al.* [1] developed a simplified model of a SOIC-8 package which treats all package grounding leads to be of equal importance. The model described in the present paper improves on [1] in that it accounts for the fact that some grounding leads are more important than others depending on where they are located. This is an important modification especially for large packages. The proposed model has a physical interpretation also in that it properly models the image current behavior on the paddle.

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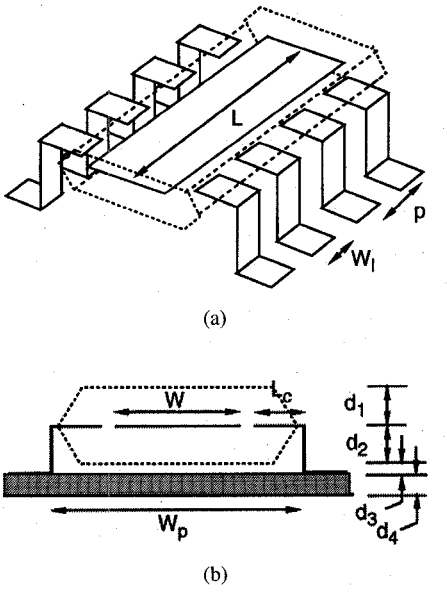


Fig. 1. Illustration of a SOIC-8 plastic package (a) perspective and (b) side view.

In this paper, we describe how one could split up the modeling of a plastic package and what circuit models could be used for each of the pieces. By splitting the over-all model, we allow the circuit designer to connect the pieces together and to a MMIC circuit in whatever way is best for the circuit operation without doing extensive full wave simulations. Splitting and reconnecting using only circuit connections assumes that all other mutual couplings are negligible. It is necessary to determine whether this is true for the split we propose. To do that we need an efficient way to simulate an entire structure leads, paddle, wire bonds, and test MMIC as one unit. The results can then be compared those from the reconnected circuit model. We do this using the three-dimensional (3-D) planar simulation package Em by Sonnet Software [2]. This is a method of moments solver that includes all electromagnetic effects. To conserve simulation time, the structure we simulate is not exactly the same as a SOIC package, but it is close and it is simple enough that we can simulate an entire package/test circuit/motherboard as a unit. If our split matches reasonably well to the over-all simulation, then the topology is verified. The simulation of each piece can then be upgraded as necessary to better match a real package.

In what follows, we describe the circuit topology used to model the package and how the components in this topology are determined from the electromagnetic simulation. The next

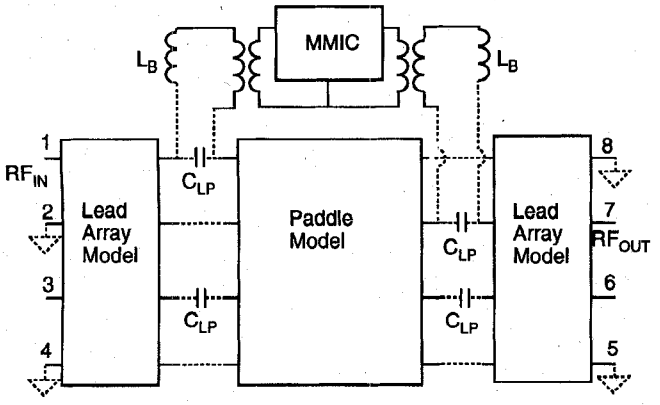


Fig. 2. Topology of the package circuit model.

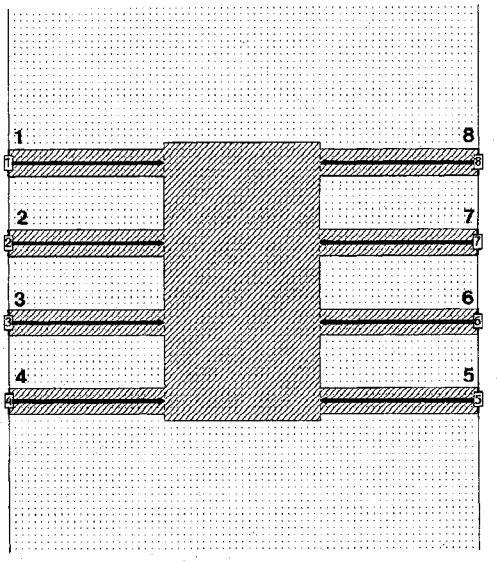
section gives an overview of the modeling scheme. Sections III, IV, and V describe the details of the component evaluation. In Section VI, the technique is applied to a test circuit housed in a SOIC-8 package and the result compared to an electromagnetic simulation of the overall circuit. The results are discussed in Section VII.

II. Overview

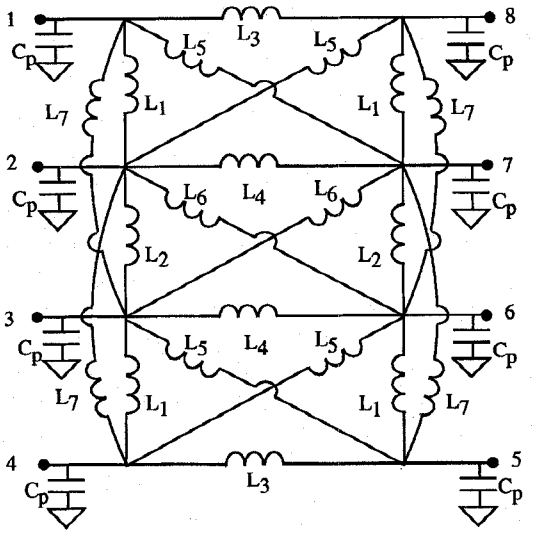
Fig. 2 shows how we split the model into three pieces: the paddle, the lead array, and the lead/paddle interconnection. The lead model obviously models the lead array illustrated by the stepped planar conductors in Fig. 1(a). The lead/paddle interconnection principally models the wire bond connecting a lead to either the MMIC or to the paddle. The paddle model models how the current returning from the MMIC distributes itself to whatever leads connect the paddle to the motherboard ground. Each piece is simulated on Em [2] and the results used to determine a circuit model. Once the circuit models are obtained, the three pieces are connected to each other and to the MMIC. Fig. 2 shows one possible interconnection with dashed lines.

By splitting the package into three, we are assuming that each of the three pieces couples to the other only through the terminal connections shown. This is an approximation since there are small capacitive and inductive mutual couplings that occur in addition. As we describe in the following sections, we approximately include these effects by the manner in which the individual pieces are simulated.

The MMIC is connected to the three piece model using the ideal transformers T_1 and T_2. These transformers force currents in the circuit model to behave approximately the way they do in a full wave simulation of the package. Plots of simulated currents using Emvu [2] clearly show that the current injected via a wire bond into a MMIC returns from it as an image current on the paddle. The image current shadows the wire bond to the vicinity of the point on the paddle edge over which the wire bond passes. It then distributes itself to the paddle ground leads by flowing, for the most part, along the paddle edge. The transformer T_1 in the circuit model forces the MMIC input current to return to the appropriate terminal on the paddle model. Transformer T_2 does the same for the output current. In the circuit model, every connection



(a)



(b)

Fig. 3. (a) Simulator layout for the paddle and (b) the circuit model.

between the MMIC and a package lead will have an ideal transformer associate with it (including power supply lines with off package decoupling).

III. Paddle Model

Fig. 3(a) shows the paddle structure simulated on Em. An eight port is created by connecting eight strip lines to the paddle at points commensurate with the location of leads. The reference planes for each port are at the paddle edge. Our assumption is that a wire bond return current traveling on the paddle to the vicinity of, for example, lead one will distribute itself to the other leads in the same way a current injected into port 1 of Fig. 3(a) distributes itself to the other ports.

Table I shows the y parameters for a simulation of a SOIC-8 paddle. Note that the transfer admittance is much larger between ports which are near neighbors than it is between ports more widely separated. This corresponds to the fact that

TABLE I
Y AND Z PARAMETERS OBTAINED FROM FULL WAVE SIMULATION AND FROM A CIRCUIT MODEL FOR AN EIGHT PORT PADDLE AT 1 AND 10 GHz. SIMULATION PARAMETERS (mm): $d_1 = d_2 = 0.635, d_3 = 0.2, d_4 = 0.25, L = 4.2, W = 2.4, W_1 = 0.406, p = 1.27, \varepsilon_1 = \varepsilon_2 = 4.0, \varepsilon_3 = 1.0, \varepsilon_4 = 10.0$, MODEL PARAMETERS: $L_1 = 0.36$ nH, $L_2 = 0.33$ nH, $L_3 = 1.9$ nH, $L_4 = 6.4$ nH $L_5 = 5.9$ nH, $L_6 = 5.1$ nH, $L_7 = -4.6$ nH, $C_p = 0.05$ pf

	1 GHz		10 GHz	
	Em simulation	circuit model	Em simulation	circuit model
y_{11}	-j 0.492	-j 0.519	-j 0.0475	-j 0.048
y_{12}	j 0.443	j 0.443	j 0.0460	j 0.044
y_{13}	-j 0.035	-j 0.035	-j 0.0038	-j 0.0034
y_{14}	-j 0.014	0	-j 0.0018	0
y_{17}	j 0.027	j 0.027	j 0.0022	j 0.0027
y_{18}	j 0.084	j 0.084	j 0.010	j 0.0083
y_{22}	-j 0.979	-j 0.982	-j 0.10	-j 0.094
y_{23}	j 0.489	j 0.490	j 0.052	j 0.049
y_{26}	j 0.031	j 0.031	j 0.0023	j 0.0031
y_{27}	j 0.025	j 0.025	j 0.0044	j 0.0025
z_{11}	-j 393.5	-j 391.6	-j 6.35	-j 12.5
z_{15}	-j 397.5	-j 395.0	-j 55.0	-j 51.7

the current flows around the edges of the paddle and suggests the circuit model described next.

The circuit model shown in Fig. 3(b) was chosen for its simplicity and its expandability. In [3], Rautio describes a technique for deriving a circuit model for a structure from an Em simulation of it. This technique was used here, but for simplicity, we neglected the transadmittance between ports that are farthest from each other (such as 2 and 5). Also, we have used only inductances between nodes and capacitances from each node to ground. So if the inductance between ports i and j is L_{ij}, then

$$L_{ij} = \frac{-1}{j\omega y_{ij}} \tag{1}$$

where, for example, L_3 in Fig. 3(b) equals L_{18} as calculated from (1). The capacitance value C_p can be determined from

$$C_p = \frac{1}{j\omega N z_{ii}} \tag{2}$$

where i can correspond to any one of the ports and N is the number of ports. Low frequencies should be used for these evaluations. In our case 1 GHz was chosen. Table I shows the agreement between the simulation and the model over a 1 decade of frequency.

The topology chosen here has a number of features. By neglecting the transfer admittance between distant ports on the paddle, the number of components in the model goes up linearly with lead number instead of as the square. Secondly, there is a great deal of symmetry in the topology and although the number of components may become quite high for large packages, the number of different component values will be much less. The most important components in the model connect adjacent ports on the perimeter. In the SOIC-8 example, this is L_1, L_2, and L_3. At frequencies high enough for the package to resonate this simplified model becomes less accurate. However, accuracy at such frequencies is less important than accuracy at lower, more useful, frequencies.

IV. LEAD ARRAY MODEL

Referring to Fig. 1, the lead arrays are the sets of conductors connecting circuitry located on the paddle plane to circuitry on the plane of the motherboard. For the SOIC-8 example, there are two arrays of four leads. The lead width and pitches are denoted as W_L and p, respectively. The other dimensions of the leads are L_c, d_1, d_2, and d_3 as denoted in the figure. We assume zero thickness for the lead contacts even though the thickness is commonly half the lead width. This last assumption is severe, but, as noted in the introduction, the lead simulation can be upgraded at a later date by using, for example, a finite element or FTDT simulation.

Fig. 4(a) shows the structure for an Em simulation of the lead array. The simulation uses layers of dielectric uniformly distributed across the simulation box as opposed to the discontinuous layers found in an actual package. The characteristics of the layers pertaining to our example can be found in the caption to Table I. Referring to Fig. 4(a), the port reference planes on the right side are located where the wire bond would connect to the lead. On the left side, the reference planes are located where the leads leave the motherboard surface. Table II shows some of the Y and Z parameters resulting from the simulation. Notice that the transfer parameter between non adjacent leads $1'$ and 3 is relatively small.

Fig. 4(b) shows the circuit model for the lead array. Both inductive and capacitive mutual coupling between leads is included. At low frequencies, the Y parameters of the array depend primarily on L_L and M and thus these quantities can be evaluated approximately from simulated Y parameters using

$$L_L = -\left\{ j\omega y_{1'1'} \left[1 - \left(\frac{y_{1'2'}}{y_{1'1'}} \right)^2 \right] \right\}^{-1} \tag{2a}$$

$$M = -\frac{y_{1'2'} L_L}{y_{1'1'}} \tag{2b}$$

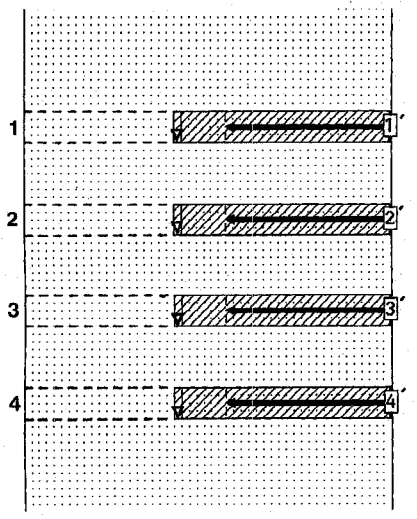
where M has been assumed to be small compared to L_L. The capacitances in the model are determined from the frequency variation in the Y parameters

$$C_2 + C_m = \frac{\left[y_{1'1'}\Big|_{\omega_h} - \left(\frac{\omega_l}{\omega_h} \right) y_{1'1'}\Big|_{\omega_l} \right]}{j\omega_h} \tag{3a}$$

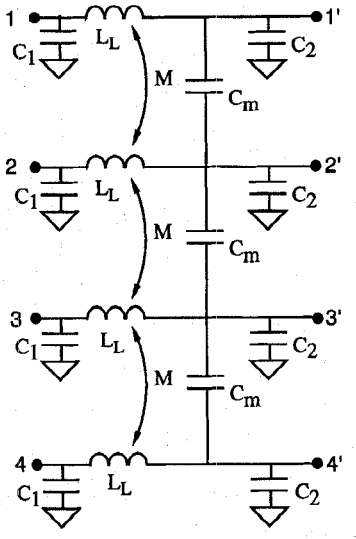
$$C_1 = \frac{\left[y_{11}\Big|_{\omega_h} - \left(\frac{\omega_l}{\omega_h} \right) y_{11}\Big|_{\omega_l} \right]}{j\omega_h} \tag{3b}$$

$$C_m = \frac{\left[y_{2'1'}\Big|_{\omega_h} - \left(\frac{\omega_l}{\omega_h} \right) y_{2'1'}\Big|_{\omega_l} \right]}{-j\omega_h}. \tag{3c}$$

Table II shows how the circuit model fits to the simulated data. Note that the circuit model neglects the mutual inductance between nonadjacent leads and thus $y_{1'3}$ is not modeled correctly.



(a)



(b)

Fig. 4. (a) Simulator layout (dashed lines drawn in to show port locations) for the basic lead array and (b) the circuit model.

TABLE II

Y PARAMETERS OBTAINED FROM A FULL WAVE SIMULATION AND FROM A CIRCUIT MODEL FOR AN EIGHT PORT LEAD ARRAY. SIMULATION PARAMETERS ARE $L_c = 0.6$ mm AND AS LISTED IN TABLE I. MODEL PARAMETERS: $L_L = 0.61$ nH, $M = 0.100$ nH, $C_1 = 0.085$ pF, $C_2 = 0.028$ pF, and $C_m = 0.0057$ pF

	1 GHz		10 GHz	
	Em simulation	circuit model	Em simulation	circuit model
$y_{1'1}$	j 0.268	j 0.268	j 0.0262	j 0.027
$y_{1'2}$	-j 0.0436	-j 0.0450	-j 0.00482	-j 0.0045
$y_{1'3}$	-j 0.00591	j 0.0076	-j 0.000653	j 0.000762
$y_{1'1'}$	-j 0.267	-j 0.268	-j 0.0246	-j 0.025
$y_{1'2'}$	j 0.0435	j 0.045	j 0.00399	j 0.0041
$y_{2'2'}$	-j 0.275	-j 0.276	-j 0.0253	-j 0.025
$y_{2'3'}$	j 0.0426	j 0.0460	j 0.00389	j 0.0042
y_{11}	-j 0.267	-j 0.0268	-j 0.0214	-j 0.021
$y_{22'}$	j 0.274	j 0.276	j 0.0222	j 0.028
y_{12}	j 0.0436	j 0.0450	j 0.00445	j 0.0045

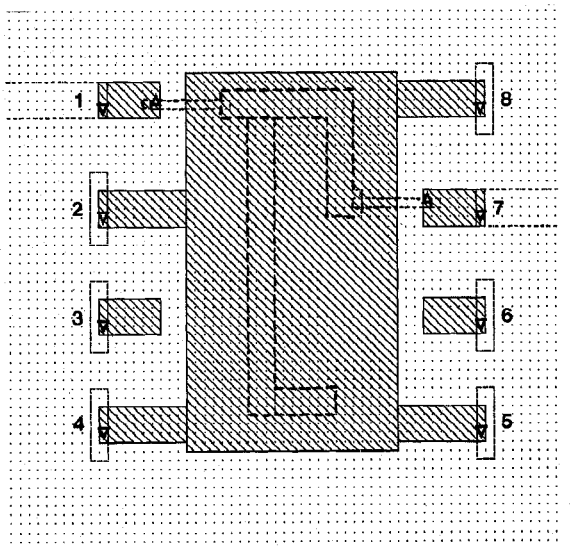


Fig. 5. Simulator layout for packaged test circuit.

The elements in the circuit model corresponding to leads that ground the package paddle must be modified from what was calculated above. The package behavior is very sensitive to the inductance of these leads, and they have a somewhat different structure than the other leads. On the paddle level, grounding leads may connect directly to the paddle thus requiring $L_c = (W_p - W)/2$ (see Fig. 1). Since such leads are longer than a wirebonded lead, there is a small additional inductance. On the motherboard level, the lead can connect with the motherboard ground in a variety of ways. In our example, we assume a via ground is located directly beneath the foot of the lead. Since there is significant mutual coupling between the via and the vertical section of the lead above it, both must be simulated as one unit. Simply simulating a via ground by itself and adding its inductance to the model described above will give inaccurate results.

The model elements for paddle grounding leads are found from the simulation of a pair of the leads in Fig. 4(a). The pair is modified by replacing the left side feed leads with vias of the form shown in Fig. 5(a) and by lengthening the paddle level lead length, L_c. The resulting 2-port Y parameters are used in (2), (3a), and (3c) to determine L_L, M, C_m, C_2. In our example, these values come out to be 0.909 nH, 0.100 nH, 0.0084 pF, 0.034 pF, respectively. These values correspond to two grounding leads adjacent to each other. In cases where a grounding lead is adjacent to a nongrounding lead, we replace the appropriate M and C_m with the average of their grounding and nongrounding values.

V. LEAD/PADDLE INTERCONNECTION

Wire bonds from a lead to a MMIC are modeled as a simple inductance which can be determined quasistatically [4]. The quasistatic evaluation has been shown to be reasonable up to the vicinity of 20 GHz [5]. In our work, we have used Em to do a simulation of a wire bond. It is not necessary to do it this way, but, as stated previously, we want to be able to simulate the entire package using Em so that we can then compare the results to our combination of circuit models.

The setup for the Em wire bond simulation is as follows. The input feedline is a microstrip of width W_L and is elevated a distance $d_2+d_3+d_4$ above the ground plane. The "wire bond" is a 0.1 mm $\times$ 0.1 mm vertical via going up 0.25 mm to a 0.7 mm length of 0.1 mm wide microstrip line followed by another via going down 0.15 mm. At this point the "wire bond" is connecting to what would, in a real package, be a 0.1 mm thick MMIC on the package paddle. In the simulation, it connects to a microstrip feedline of width W_L extending in a direction perpendicular to the wire bond. From the simulated 2-port Y-parameters, we calculate $L_B = 0.59$ nH. We emphasize that this inductance is not necessarily the same as the inductance of a standard 25 um bond wire with an irregular shape. We are only using it to test our modeling algorithm.

In the simulation, the lead side of the wire bond is fed by a line which is parallel to it while the paddle side is fed by a perpendicular feed. The reference planes on both sides are at the wire bond ends. The parallel feed is used so that the apparent inductance of the wire bond includes the effect of the mutual inductance between the feed and the wire bond. This approximates the coupling that occurs in the actual package. The apparent inductance of the wire bond increases substantially (20% in our examples) due to this coupling. On the other end of the wire bond, a perpendicular feed is used in order to eliminate any feed-wire bond coupling. This again approximates the packaged situation where the paddle side of the wire bond attaches to the microstrip in the test circuit. Due to the canceling effect of the paddle image currents, the microstrip test circuit will not couple strongly to the wire bond.

In many plastic packages, the paddle end of a lead is close to an edge of the paddle (0.2 mm in a SOIC package). This introduces capacitive coupling between the lead and the paddle which we have designated as C_{LP} in Fig. 2. Our modeling has shown that this capacitance has a significant effect on package resonance frequency. We have determined values for this capacitance from simulations of gap coupling between a microstrip line with the same width as a feed line (W_L) and a very wide microstrip line. The capacitance so determined ($C_{LP} = 0.053$ pF) is likely to be much less than in an actual package since the gap used in the simulation (0.3 mm) is more than in an actual package (0.2 mm) and the metallization thickness in the simulations (zero) is much less than in an actual package (0.2 mm).

VI. Test Case

Fig. 5 shows a test case where a test circuit is placed in the package we have been modeling above. The test circuit is a two port consisting of a length of microstrip having a open circuit stub attached. The traces have widths of 0.3 mm, are elevated 0.1 mm above the ground plane, and are embedded in an $\varepsilon_r = 4$. layer of thickness $d_1 = 0.635$ mm. One port of the test circuit is connected to lead 1 of the package and the second port is connected to lead 7. Leads 2, 4, 5, and 8 connect the paddle to motherboard ground with vias through layer 4 (see Fig. 1). Leads 3 and 6 are grounded to the motherboard, but not otherwise connected. Since Em is not capable of doing irregular dielectric structures, all layers extend across the entire

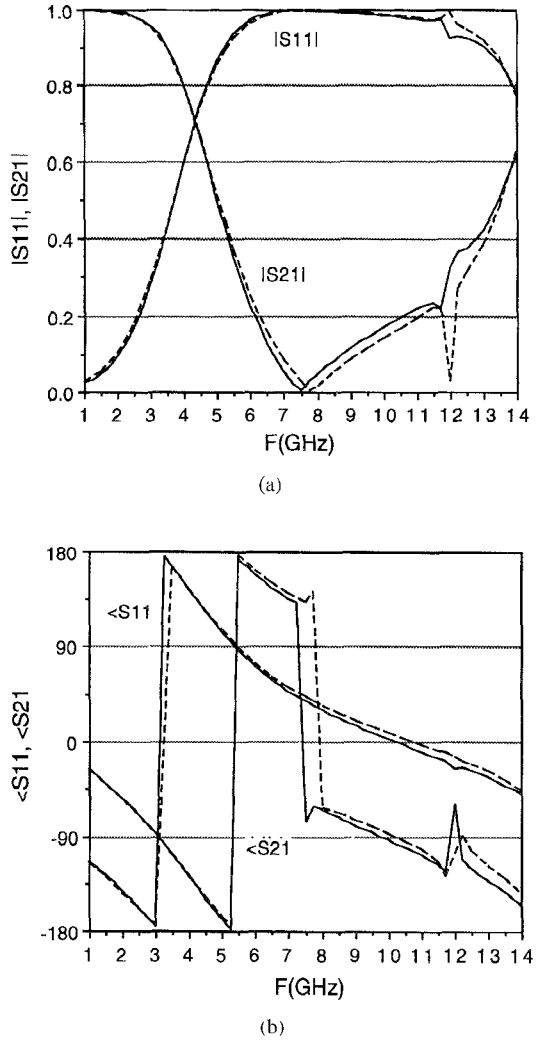


Fig. 6. (a) Magnitude and (b) phase of S parameters for the packaged test circuit as computed from the circuit model (solid line) and full simulation (dashed line).

simulation box. The dashed lines in Fig. 6 show the scattering parameters resulting from the simulation of the entire structure. Note that there is a zero of transmission at 7.75 GHz and a package resonance at about 12 GHz.

Next, the same structure is simulated using the circuit models we have developed in the preceding sections. The electrical characteristics of the block labeled MMIC in Fig. 2 are described by multifrequency S parameter data generated by simulating the unpackaged microstrip/stub two port. By unpackaged, we mean only the through line and stub with no package involved. This data has not been included with this paper, but it is important to note that it shows a transmission zero at 9.5 GHz where the stub becomes one quarter wavelength long. In the unpackaged circuit simulation, the input and output feed lines are the same as the microstrip in the circuit being simulated and the reference planes are located where the wire bond would connect in the package.

The circuit model of the packaged structure produces the S parameters denoted by solid lines in Fig. 6. In most cases the agreement with the full wave simulation would be considered acceptable over a broad frequency range. Note that packaging the test circuit has a huge effect on the frequency

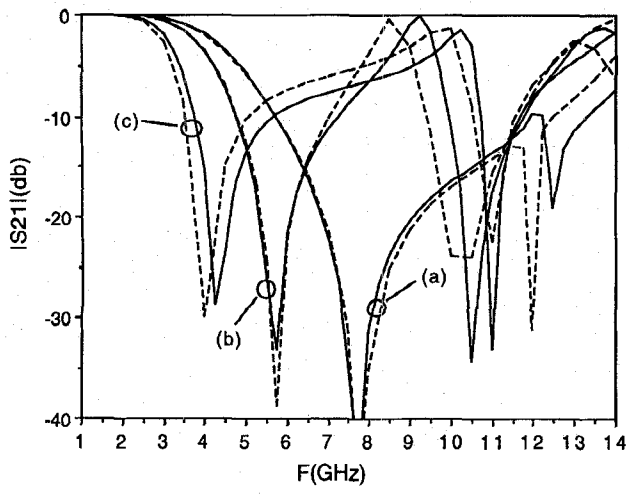


Fig. 7. $|S_{21}|$ versus frequency for the packaged test circuit as computed from the corrected circuit model (solid line) and full simulation (dashed line) under the conditions: (a) leads 2, 4, 5, 8 are grounded, (b) leads 2, 8 are grounded, and (c) leads 4, 5 are grounded.

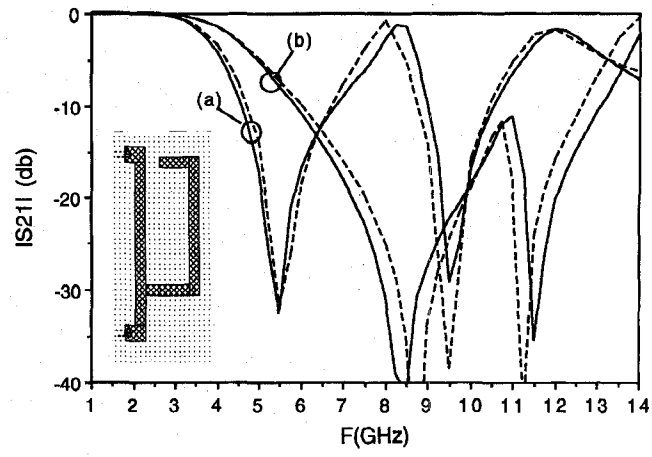


Fig. 8. $|S_{21}|$ response for a thru/stub test circuit(see inset) connected between leads 1 and 4 under the conditions (a) leads 2, 3 are grounded and (b) leads 2, 3, 5, 8 are grounded. Solid and dashed lines denote results computed from the circuit model and simulation, respectively.

of the transmission zero, shifting it from 9.5 GHz in the unpackaged case to 7.75 GHz when packaged. The circuit model accurately models this shift, showing a transmission zero at 7.50 GHz—lower by 3% than in the full simulation.

The sensitivity of $|S_{21}|$ to the various circuit elements has been investigated. At 4 GHz, the largest sensitivity is that of the lead inductances, L_L, that ground the paddle. The next largest sensitivities correspond to the wire bond inductance, L_B, and the paddle inductance, L_1, but these are 80% less sensitive than L_L. At 9GHz, L_L still has the highest sensitivity, followed by the paddle capacitance, C_p, and L_B. The latter two are only 30% less sensitive than L_L. C_p has gained in importance.

To further refine our circuit model, we changed our test circuit to one with a via short in place of the stub. We full wave simulated the entire structure and compared the results to the circuit simulation with the MMIC block changed as appropriate. We then optimized L_L, L_B, C_p so as to fit the circuit model Y parameters to the Em simulated Y parameters over a range of frequencies. These three elements changed slightly from {0.91 nH, 0.59 nH, 0.050 pF} to {0.87 nH, 0.57 nH, 0.041 pf}. This type of adjustment procedure is what one might use if experimental results were available in place of the electromagnetic simulations. All the circuit model results that follow use the adjusted L_L, L_B, C_p.

Fig. 7 shows the $|S_{21}|$ frequency response for circuit simulations of three grounding configurations. When leads 2, 4, 5, and 8 via ground the paddle to the motherboard, we have the same configuration as for Fig. 6, except that aforementioned adjusted components are used. The transmission zeros of the circuit modeled and fully simulated structures are right on top of each other at 7.75 GHz. The agreement between modeled and simulated phase of S_{21} are similarly improved from Fig. 6. Also shown are the circuit and full wave results when only leads 2, 8 ground the paddle and when only leads 4, 5 ground the paddle. Removing grounds moves the transmission zero away from its unpackaged value of 9.5 GHz. In the first two cases, the circuit and full wave simulations agree very well up to frequencies near the package resonance. In the third case, the grounds are located at the opposite end of the package from the signal lines. The agreement between the two simulations is less good—probably due to the simplified paddle model we used. The transmission dips caused by the package resonances agree roughly with the full wave analysis. Of course, the circuit simulation takes a fraction of the time needed for the full wave result.

Note that the transmission zeros when leads 4, 5 are grounded is shifted by about 1.5 GHz from the transmission zero when leads 2, 8 are grounded even though the same number of leads are grounded in both cases. The location of the grounding leads is therefore important. Some of this shift is due to the reduction in mutual coupling between the leads (labeled M in Fig. 4) when the leads are more separated, but this is not sufficient to explain the majority of the shift. Setting M to zero in the circuit simulation only moves the transmission zero down by 0.5 GHz—only 30% of the total shift. The remaining shift is due to the extra distance the current travels along the paddle edge when pins 4, 5 are the grounds.

Lastly, a different stub/thru circuit is connected between leads 1 and 4. The test circuit is shown in the inset to Fig. 8 and has an unpackaged transmission zero at, again, about 9.5 GHz. Fig. 8 shows the circuit modeled and full wave simulated $|S_{21}|$ for two different ground lead connections. The package model components used to get the results in Fig. 8 are the same as the ones used for the results in Fig. 7 except that the elements for the grounding leads have been shifted around as appropriate.

VII. Discussion

An important part of this modeling scheme is the assumption that the bond wire current crossing a paddle edge passes through the MMIC, returns on the paddle beneath the bond wire to the edge of the paddle, and is then distributed to the paddle grounding leads. Plots of the image currents on the paddle clearly show this effect. This behavior leads to

the transformer based circuit topology since it emphasizes the importance of ground lead location.

There are several common situations that can easily be modeled with this approach. For example, if a MMIC has a part of its circuit grounded to the paddle with a wire bond, the modeling of this connection falls inside the box labeled MMIC in Fig. 1. There is no transformer involved since there is no off-paddle connection. Another common situation occurs when two MMIC's are mounted on the paddle and wire bonded together. Again, the modeling of them and their interconnection are included within the MMIC box in Fig. 1. Their interconnection would be modeled as if there were an ideal ground plane of infinite extent supporting the MMIC's. Only where currents cross the paddle edge and connect to a lead would a transformer be placed and connections made to the package model.

In some cases, a wire bond connecting a lead to a MMIC will be long enough to travel a significant distance over the paddle. Beyond a certain point the image currents in the paddle become well formed and the model of that section of the bond wire should be included in the MMIC block. In other words, we visualize a boundary located just within the boundary of the paddle. Structures inside this boundary—MMIC's or wire bonds—have well formed image currents. Their models would be included in the MMIC block and would come from simulations with an ideal ground plane assumed. Outside the boundary, the image currents of the bond wires appear in the ground plane of the motherboard, much farther away. Those parts of the bond wire are modeled as described in Section V. The transformer connects the two models across the boundary. The location of this boundary is somewhat vague. We have chosen it to be about 0.4 mm inside the actual boundary based on our observations of current distributions on the paddle. In the test cases described in the last section, the bond wires were relatively short and were assumed to be entirely outside the imaginary boundary.

The network used for modeling the paddle has been kept relatively simple so that it can be expanded for use with 16 or 24 pin packages. This simplicity results in loss of accuracy when operating at frequencies near a package resonance and when grounding leads are distant from signal leads.

VIII. Conclusion

A scheme for modeling plastic surface mount packages has been described. It consists of three parts which can be simulated separately, converted to circuit models, and connected together for use in standard circuit simulators. It should be emphasized that the detailed modeling procedure described herein only has to be done once for a given package type. It can then be used by designers to investigate various lead connections to the packaged MMIC(s) or to paddle ground. Fundamental to the modeling technique is the use of ideal transformers to properly direct the current return paths from the MMIC to motherboard ground. This topology improves on previous models by accounting for the importance of ground lead positioning. We have tested our modeling procedure by comparing S parameters from the three part circuit model to a full wave simulations of an entire SOIC-8 packaged test circuit.

References

[1] F. Ndagijimata *et al.*, "The inductive connection effects of a mounted SPDT in a plastic SO8 package," in *IEEE Microwave Theory Tech. Symp. Dig.*, June 1993, pp. 91–94.

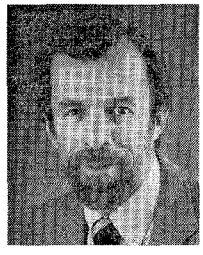
[2] Em and Emvu are trademarks of SONNET Inc., 135 Old Cove Road, Suite 203, Liverpool, NY.

[3] J. C. Rautio, "Synthesis of lumped models from N-port scattering parameter data," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 3, pp. 535–537, Mar. 1994.

[4] F. W. Grover, *Inductance Calculations: Working Formulas and Tables.* New York: Dover, 1973.

[5] H. Y. Lee, "Wideband characterization of mutual coupling between high density bonding wires," *IEEE Microwave Guided Wave Lett.*, vol. 4, no. 8, pp. 265–267, Aug. 1994.

[6] S. K. Yun and H. Y. Lee, "Parasitic impedance analysis of double bonding wires for high frequency integrated circuit packaging," *IEEE Microwave Guided Wave Lett.*, vol. 5, no. 9, pp. 296–298, Sept. 1995.



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